Improved Leakage Power Fall Technique of CMOS VLSI Circuits and It's Design and Execution

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Abstract: The fast increment of semiconductor innovation and developing interest for versatile gadgets controlled up through battery has driven the constructors to downsize the element size; resultant diminished edge voltage just as accordingly empowering joining of fantastically complex usefulness on a solitary chip. In both mechanical and usage viewpoints Chip's greatest force approach is received. To build the show of gadgets, the three key variables are basic, for example, speed of the framework, little territory, and low force utilization. In particular, in the coordinated gadgets all out force utilization is affected by the spillage current dispersal. For superior applications with negligible voltage and force decrease of spillage power is of significant concern. Force spillage minimization request might be because of quick improvement of intensity electronic gadgets worked in batteries like mobile phones, workstations, and other handheld gadgets. In the close past, a large number of them have centred towards handling the issues and still in progress. In this exploration will contemplate and examine the spillage segments. Moreover, proposed another upgraded spillage power decrease method by the blend of Sleepy stacked with LECTOR strategy. This incorporates two spillage control transistors included between the draw up and pull down circuit .The stack impact will be presented through subbing each current transistor with two half estimated transistors. It conveys the restriction of the zone in view of use of additional transistors towards saving the circuit state during rest mode. Additionally, embedding high opposition between the gracefully and ground by methods for CMOS switch. This procedure will give phenomenal spillage current decrease immediately punishment.

Keywords: Power Consumption, CMOS, LECTOR, Current Reduction

INTRODUCTION

In this cutting edge world, because of progression of battery-based gadgets with restricted force abilities needs significant necessity of intensity proficiency and force postpone item. These two variables are of extraordinary test to the electronic originators [1]. Correspondingly, in VLSI circuit configuration power utilization of circuit is of significant concern. The interest for low force gadget isn't a direct result of improvement of portable application alone [3]. The issue of intensity utilization is significant issue before the development of versatile time. To determine power scattering issue various strategies and techniques has been proposed by scientists as far as building, gadget level and even some more significant levels. Till today there isn't standard methodology is advanced for elements to conquer issue of zone utilization, deferral and force use of the structured circuit. In view of the item and application prerequisite client need to choose most fitting strategy. If there should arise an occurrence of elite compact gadgets power dispersal is the significant concern.

Three parts assumes imperative job for power utilization which are all spillage current, short out and dispersal of intensity from dynamic exchanging [4]. In CMOS circuit complete force scattering turns into a predominant segments in view of consistent scaling of limit voltage [5]. Through the reusing of put away vitality in the hubs dynamic scattering get decreased in adiabatic registering. Indeed, even in adiabatic procedure dissemination of vitality happened for consistent information esteems. Nonetheless, vitality scattering happens

in any event, for steady info signs of the adiabatic circuits where power-timekeepers are utilized for charging and releasing of yield hubs [6]. Because of consistent scaling in CMOS innovation in adiabatic procedure dissemination because of spillage in the circuit configuration will proceed as predominant segment for in general scattering of intensity same as customary rationale capacity of the CMOS gadgets. In adiabatic circuit power gating approach is received for limiting spillage and dynamic intensity of the framework. In this procedure out of gear state power gating framework shut down the units. The adiabatic circuit is essentially varying from CMOS circuit because of sign waveforms and checking plans in traditional methodologies. In this plan it is vital that there should be sufficient recognize switch with Power-gating and power clock used for killing. In adiabatic plans different force gating are applied [6], [7].

Among the numerous gating approaches voltage scaling approach outperforms in case of adiabatic based CMOS logic circuits. In the mid performance ranges from (5MHz to 100MHz) supply voltage scaling in medium-voltage region performs effectively [8]. Based on this numerous adiabatic –circuit with near-threshold has been proposed without the use of gating power. Due switching power dissipation is minimized to quadratic in this scenario minimization of power consumption by the use of supply voltage technique. This technique has the serious issues of performance degradation. Sub sequent, the high performance requirements were fulfilled by scaled value of threshold voltage. This technique has the serious drawback of increased leakage current which put forth the major concern for high performance circuit with low power utilization [9]. In this paper, proposed a new approach, thus providing a new choice to low leakage power VLSI designers. Furthermore, summarized the existing approach as well as identified the issues towards power reduction.

RELATED WORK

In existing, most of them have suggested a different method towards control leakage power consumption. These are discussed as follows: Few of them have focused on sleep transistor approach [10]–[13]. In the sleep mode through the power cutting off sleep transistors will be turned off. Though this approach the leakage power reduced in the power source by cutting off in the circuit design. However, this results in the destruction of state plus a floating output voltage in sleep mode. Additionally, this approach reduces delay through the sleep mode sleep minimization by increasing the wake up time to maximum. In existing literatures [12], [14] sleepy stack approach is developed. Through the stack effect transistors in sleepy stats are divided in to two separate half-length transistors for the designed sleepy state design. These classified transistors are parallel connected to the one of the transistor which acts as a dividend. In sleep mode/ saving state, leakage current are suppressed by stacked transistor through turning off the sleep transistor. In this technique product penalty of power delay plays significant role since where every transistor is replaced with three transistors. Sleepy stack approach is formed with the combining of transistor stacking with sleep approach for mitigating of sub threshold leakage current reduction [15], [16].

During stacking transistor is divided into two half of pull up and pull down the network which increases the resistance of circuit and sleep transistor connected paralleled which exponentially reduces the I SUB , main advantage of this circuit is that it maintain the proper logic of the circuit without rail out from V dd and main disadvantage of approach is that we cannot use high Vth transistor for further reduction of leakage power [17].Dual sleep

technique [18]uses either ON or OFF mode in the sleep mode by incorporation of two pull-ups and pull-down individually. Through which dual sleep portion can be made common for the entire circuit design where some logic circuit requires transistors in minimal count[19], In comparison with existing researches it needs increased power delay which may impact on increase in delay of the circuit.

DESIGN PROCEDURE

Nowadays, the design of low power circuit has developed as the main topic in the electronics industry. Subsequently, the requirement of this low power has created a noteworthy outlook change, whereas the dissipation of power is a significant factor for deliberation of area and performance. This this section presented anew leakage power reduction techniques and corresponding simulation were presented. These are discussed as follows.

A. Proposed method

In this study, proposed a novel technique that reduces the power leakage of the VLSI circuit design with CMOS circuit. The new approach is sleepy stacked with LECTOR transmission approach. The circuit diagram is shown in figure.2.The proposed scheme uses aspect ratio of W/L=2 in case of PMOS circuit transistor. In other case of NMOS transistor the aspect ratio is of W/L = 1. Through the minimal aspect ratio of the circuit sub-threshold value get minimized.

In this technique, the sleep transistors are used for differentiation of ground and power supply. Other than those remaining transistor are connected to gate. It depends on input vector and controls the switching of sleep transistors, consuming power in both active and idle states. Furthermore, the two transistors are added in logic circuit based on the Pull- up and pull-down design network circuit. To cope with input combination are connected in transistor by placing any one of the transistor near the cut-off voltage. This transistor design will provides the path resistance for ground to supply connection. This resistance will provides minimized leakage current in the circuit. The designed circuit will performs effectively for the both active and standby mode of the circuit design. Furthermore, increase the resistance in the path from source to ground.

The system array is designed using transistors VCC and GND terminals. Such an arrangement is called as self-controlled voltage technique. It is implemented such that it reduces the amount of power consumption by allowing the transistors to swing between safe voltage values to prevent excess power consumption. As the leakage current reduces, the power dissipation across the transistors is also reduced significantly.

B. Layout Design

The layout design of transistors shows the implementation of NMOS by n+ gate and diffusion layer through the incorporation of poly-silicon. Further the designed circuit interconnected with metal-1 and metal-2 for implementation. In this designed circuit read and write operation will be performed for the active word line in the circuit. The designed circuits act as open circuit when word line is not on active state. The below figure 1 illustrates proposed architecture design which contains LECTOR stack for power consumption. This proposed approach uses a combination of Pull Up and Pull down logic design for power consumption minimization. The sleepy signal is fed in to Vcc with parallel connection with Pull Up and Pull down logic circuit were in both the transistor is provided with the sleepy

signal waveform. Implementation of the proposed approach is adopted in VLSI circuit design, and corresponding performance is analysed.

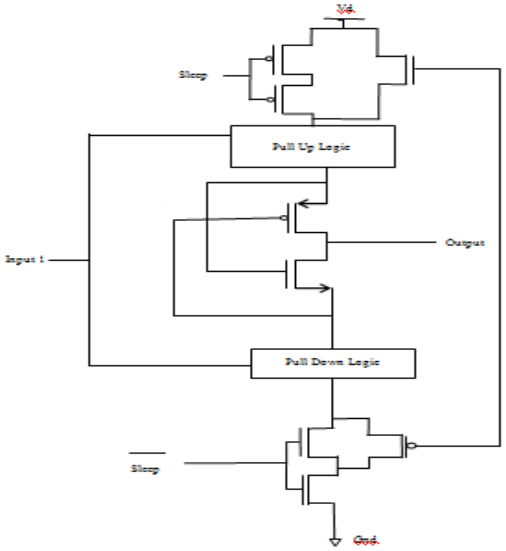

Figure 1. Block Diagram of proposed method

OPERATION PRINCIPLE

The sleep signal incorporated in the design turns off the certain parts of the circuit which are not used and turned off in the simple and fast way. When the design part activated or start connecting leakage current will be minimized in huge amount which means there will not be huge leakage current. In sleep mode signal provides the critical part to identify the sleep mode signal need to be transferred without altering the other part of the design by minimizing threshold currents. In the case of active mode of the device sub-threshold, current need not be concerned since the current in the circuit design is dynamic. The proposed design is based on the considering this factors for minimizing leakage current reduction. In proposed design circuit the main concept is charge sharing and recovering of stored charges between output capacitor and capacitance nodes. In recharge phase of the proposed circuit design the charging and discharging of the node is performed by setting it at VDD/2. Further the charging and discharging is performed for the voltage ranges from VDD/2 to VDD or in the range of VDD/2 to 0 respectively for the designed circuit. The voltage power at the rate which is half the power of VDD ideally minimizes consumption of active power up to 50%. By the incorporation of scaling in the designed technology the impacts are channel length reduction, leakage current, threshold voltage, and leakage power are the dominant portion of the power in wider gates increased dramatically. Through the evaluation of designed circuit, it is clearly observed that to eliminate the sub-threshold current voltages in the source and drain need to be equal. The proposed design is developed to operate in two modes of operation like active and sleep mode.

A. Active mode

For the design circuit input and output signal of the system are in the range of VDD/2 to 0 and VDD/2 to VDD respectively. In the evaluation phase of the circuit design, all nodes in the circuit design are in the range of VDD/2 for pre-charge phase, and output of the design

circuit is ranges from VDD/2 to 0.In the designed network topology it provides faster NAND gate operation without considering any skew of the signal, through the utilization of domino logic function in the connected transistor in the designed pull-down network. In the proposed topology evaluation phase varies from VDD/2 to for the output voltage in the pulled down circuit from VDD/2 to 0. The output node voltage V0 in the pulled down transistor remains the voltage value of VDD/2 and vice versa.

B. Sleep mode

In sleep mode, evaluation phase is disabled after the pre- charge phase of the proposed design. Every nodes proposed design all nodes have the power values are at the rate of VDD/2 in the evaluation phase. When high-level latches are located in the evaluation phase sub-threshold current may decrease drastically which is considerably small in the case of drain-source voltages.

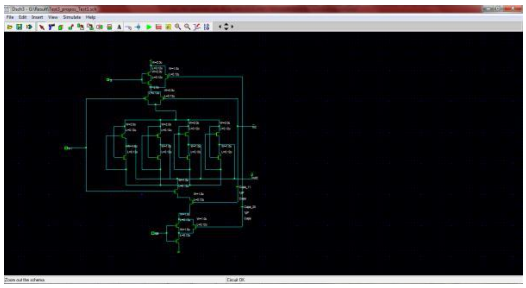

Figure 2. Logic diagram of proposed method

The proposed design is simulated using micro wind software with various technologies, and the results are depicted. This layout design contains cascade connection of proposed Sleepy stacked with LECTOR approach were implemented. In this layout design, transistor logic circuits are provided with constant input voltage supply for the both pull-up and pull- down transistors. In designed layout individual pull-up transistors are provided with 0.12V and 2.0V supply with a capacitance value of 1pF.

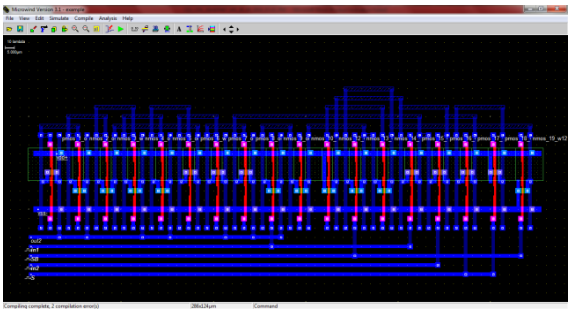

Figure 3. Layout design of proposed method

Layout design for proposed approach is shown in figure 3. This contains 10series connection of NMOS devices for same input power level .Further, this layout design contains 8 PMOS transistor for transmission of a signal in cascade. In layout design PMOS_15 and NMOS_9 is designed as In1 circuit for processing electrical signal and PMOS_ 16 and NMOS_10is selected as Input 2 for the developed architecture design circuit. From the output signal waveform is obtained for the feed input power supply, and the sleepy

waveform is applied to the transistor.

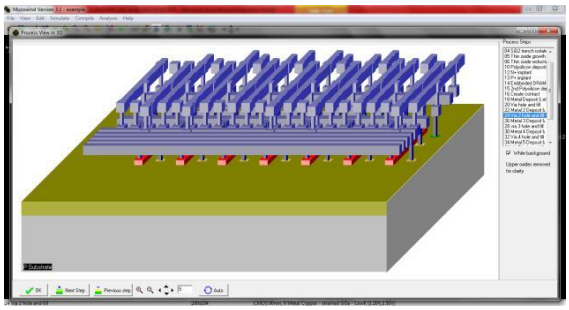

Figure 4. 3D view of proposed method

The design was tested with varying voltage and current levels at the inputs. To test the effect of time delay, tested the circuit at different time intervals and observed the readings. The proposed approach provides the advantage of minimized number of pins through the generation of memory in subsequent amount.

SIMULATION RESULTS AND DISCUSSION

This section provides the description of simulations of the proposed methods are elaborated and shown in tabular form. First, make a schematic diagram (Figure.2) and create a layout diagram (Figure.3)by using the tools. Secondly, obtain the results regarding power dissipation, current, and voltage. Subsequently, two type of window is involved in this tool such as DSCH and MICROWIND where layouts are designed and the parameters are power dissipation, current and voltage at different technology. For the designed circuit Verilog file is created and schematic is created. In next stage created Verilog file is compiled in MICROWIND software for evaluating performance of the designed circuit. In other words the created schematic in the Verilog is converted and generated in MICROWIND for evaluating the simulation performance of the system in Verilog files of the designed system. The simulation is carried out for the technology of 32nm, 45nm, 65nm and 90nm. The designed circuit is incorporated with the input voltage of 1.2Vwith the designed temperature of 27˚C. For the designed input voltage and temperature the transient analysis uses 10µs. Figure 5 shows the output of proposed circuit.

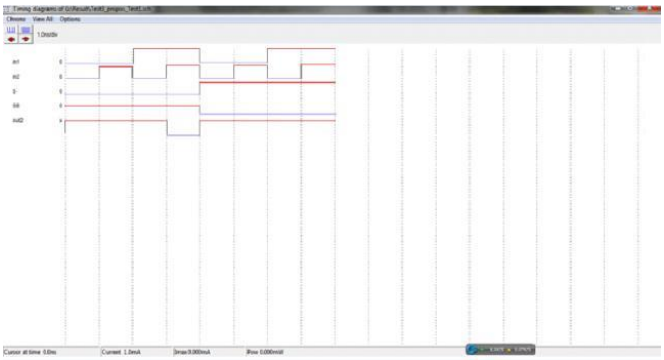

Figure 5. DSCH output result

Table 1. Simulation Data of single stage power reduction approach for NAND Gate

Techniques	90 nm	65 nm	45 nm	32 nm
Voltage	1.2V	0.7V	0.4V	0.35V
Current	0.012mA	0.08mA	0.002mA	0.003mA
Power	0.375µW	0.037 µW	0.112 µW	0.070 µW
Performance	Good	Good	Good	Good

CONCLUSION

This research article presented a technique for effective leakage power reduction in VLSI. We have applied LECTOR stack state retention with sleepy transmission approach to the NAND gate circuit. The designed circuit is comparatively analysed in terms of static and dynamic performance. Further the analysis is carried out by power-delay and propagation delay of the system with existing literatures. This approach shows effective performance for both static and dynamic power conditions. This technique provides alternative options for CMOS designer for design of circuit for significant performance. As compare to 90nm technology the circuits designed in 45nm technology produce improved results in terms of minimized power consumption rate, consumption of area and delay which make it simple and efficient for VLSI hardware implementation.

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